

Claims

What is claimed is:

- 1 1. A 3-D graphics chip having embedded DRAM buffers, the chip comprising:
2 an embedded DRAM partitioned into drawing buffers;
3 a 3-D drawing engine configured to concurrently access the embedded drawing
4 buffers for providing rendered 3-D drawing information; and
5 output means permitting the graphics chip to output the rendered 3-D drawing
6 information.
- 1 2. The 3-D graphics chip as set forth in Claim 1, further including the drawing
2 engine implementing concurrent drawing processes, the drawing processes being
3 interrelated in a predetermined manner.
- 1 3. The 3-D graphics chip as set forth in Claim 2, further including a plurality of
2 independent read FIFO's and write FIFO's used by the concurrent drawing processes to
3 access the embedded buffers.
- 1 4. The 3-D graphics chip as set forth in Claim 3, further including an access priority
2 engine, communicating with all FIFO's needing access to a given drawing buffer, and
3 granting access priority in a dynamic manner to each such FIFO, one-at-a-time, thereby
4 insuring that each concurrent drawing process obtains needed buffer access.

1 5. The 3-D graphics chip as set forth in Claim 4, further including a wide bandwidth
2 access bus for connecting a FIFO having the granted access priority with the
3 embedded DRAM.

1 6. The 3-D graphics chip as set forth in Claim 1, further including the embedded
2 DRAM being arranged in at least two independent memory banks, and each memory
3 bank having a separate wide bandwidth access bus, and each access bus having a
4 corresponding access priority engine communicating with the FIFO's.

1 7. The 3-D graphics chip as set forth in Claim 6, further including a plurality of
2 programmable switches, and each FIFO being connectable to a selected access bus
3 and a corresponding access priority engine via the programmable switches.

1 8. The 3-D graphics chip as set forth in Claim 7, further including at least two
2 drawing buffers located within a single memory bank, and the FIFO's for the
3 corresponding drawing processes being connected to the access bus and the priority
4 engine for said memory bank via the programmable switches.

1 9. The 3-D graphics chip as set forth in Claim 7, further including means permitting
2 a host device to program said switches for configuring the drawing processes via
3 FIFO's to drawing buffers in selected memory banks.

1 10. The 3-D graphics chip as set forth in Claim 4, further including each FIFO having
2 its own address register and offset register permitting each FIFO to access the entire
3 address space of the embedded DRAM.

1 11. The 3-D graphics chip as set forth in Claim 1, further including a separate
2 external memory access bus permitting at least one drawing buffer to be located in an
3 external memory.

1 12. The 3-D graphics chip as set forth in Claim 1, further including means permitting
2 a host device to initialize the contents of a drawing buffer.

1 13. The 3-D graphics chip as set forth in Claim 1, further including means permitting
2 a host device to initialize the 3-D drawing engine.

1 14. A 3-D graphics system using embedded buffers and fabricated on a single
2 substrate, the system comprising:
3 an embedded DRAM partitioned into drawing buffers;
4 a 3-D drawing engine implementing concurrent 3-D drawing processes using and
5 updating drawing information stored in the drawing buffers;
6 a plurality of independent read FIFO's and write FIFO's permitting the concurrent
7 drawing processes to access the contents of the drawing buffers;
8 a wide bandwidth access bus for connecting the independent FIFO's with the
9 embedded DRAM;

the concurrent drawing processes being interrelated such that the buffer contents are acted upon in a predefined read sequence and such that updated drawing information is produced in a predefined write sequence;

the concurrent drawing processes withdrawing the accessed drawing information from the read FIFO's according to the predefined read sequence;

the concurrent drawing processes placing updated drawing information into the write FIFO's according to the predefined write sequence;

each read FIFO independently filling with accessed drawing information at a rate permitted by the wide-bandwidth access bus and competing FIFO's;

each write FIFO independently emptying of updated drawing information at a rate permitted by the wide-bandwidth access bus and competing FIFO's; and

an access priority engine communicating with each read FIFO and with each write FIFO for resolving drawing buffer access competition by permitting each FIFO to use the wide-bandwidth access bus for accessing the embedded drawing buffers, and to insure that no FIFO is denied needed access,

whereby the 3-D graphics system throughput is maximized without incurring I/O pin limitations required for wide-bandwidth external drawing buffers.

15. A 3-D graphics system using embedded buffers and fabricated on a single substrate, the system comprising:

a 3-D drawing engine implementing concurrent 3-D drawing processes;

first and second embedded DRAM used for drawing buffers;

5 a plurality of read FIFO's used by the concurrent drawing processes for fetching
6 information from the drawing buffers;

7 a plurality of write FIFO's used by the concurrent drawing processes for storing
8 information into the drawing buffers;

9 a plurality of programmable switches configurable for connecting the FIFO's for a
10 specific drawing process to a selected embedded DRAM;

11 each DRAM having a corresponding access priority engine for determining
12 access priority among FIFO's competing for access to the corresponding DRAM.

1 16. The 3-D graphics system as set forth in Claim 15, further including external bus —
2 means for connecting FIFO's to an external memory for implementing an external
3 memory drawing buffer.

1 17. The 3-D graphics system as set forth in Claim 16, wherein the external bus
2 means includes an access priority engine for determining access priority among FIFO's
3 competing for access to the external memory.

1 18. The 3-D graphics system as set forth in Claim 15, further including means
2 permitting a host device to program the configurable switches for connecting the FIFO's
3 to selected drawing buffers.

1 19. The 3-D graphics system as set forth in Claim 15, further including means
2 permitting a host device to initialize the contents of a drawing buffer.

1 20. The 3-D graphics system as set forth in Claim 15, further including means
2 permitting a host device to store drawing engine control information in a portion of one
3 embedded DRAM and defining a control buffer.

1 21. The 3-D graphics system as set forth in Claim 20, further including the 3-D
2 drawing engine responsive to control information stored in the control buffer.

1 22. The 3-D graphics system as set forth in Claim 20, wherein the drawing engine
2 control information defines a display list buffer storing geometric attributes of 3-D
3 graphics.